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Cloud computing drives data-centre development

Packet optical: the time is right **p11**

Building tomorrow's routers today **p14**

100G demands new test strategies **p23**

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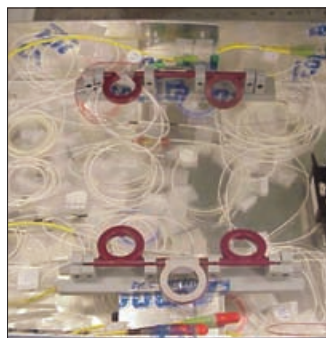
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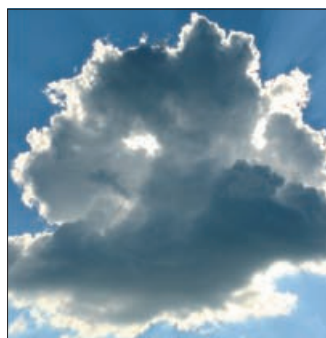
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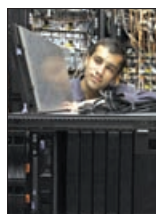
Wired: Australia plans to connect 90% of households with fibre. p7



Optics inside: researchers try to build an optical packet router. p14



Bright forecast: cloud computing is more than just vapourware. p19



On the cover: IBM is making a big push into cloud-based services. p19
Photo: IBM.

5 COMMENT

Still too crowded

7 NEWS

● Australia unveils €24 bn broadband plan ● Letter to the editor: UK fibre taxation ● Huawei takes the lead in optical ● News briefs

9 ANALYSIS

● Optical switches: set for revival ● Start-up brings integration home ● Component makers turn to outsourcing

11 OPINION

Packet optical is no 'god box'

David Dunphy assesses the prospects for packet optical transport platforms, and whether they might suffer the same fate as the 'god boxes' of the telecoms boom era.

14 RADICAL PHOTONICS

Mission possible: the all-optical router takes shape

Leontios Stampoulidis and Efstratios Kehayas describe how the European consortium ICT-BOOM is bringing the prospect of photonic routers a step closer to reality.

19 NETWORKS

Cloud computing: when telecoms and IT collide

IT directors worldwide are considering whether it makes financial sense to move their computing resources offsite into the 'cloud'. Roy Rubenstein considers the impact.

23 PRODUCT FOCUS

A new look at complex modulation

Test vendor launches what it claims is the first analyser designed specifically for advanced modulation formats.

25 PRODUCTS

- GEPON module design boasts laser monitoring
- Acrylate coating keeps working even when hot
- Collimators shine light on optical connections
- Next-generation DCMs enable flexible designs

Mission possible: the all-c

Greek researchers Leontios Stampoulidis and Efstratios Kehayas describe how the European consortium ICT-BOOM will bring the prospect of photonic routers closer to reality.

IP RULES, BUT despite this fact it is becoming very (bandwidth) hungry. IPTV, VoIP, HDTV and all the sophisticated IP-based services are causing internet traffic to more than double every year. Until recently, electronic routers have kept up with the demands in traffic growth. However, in view of the exploding capacity requirements of packet-based networks, system vendors have been forced to design “from scratch” the next generation of electronic routing systems as they prepare their next-generation of packet core networks.

The introduction of the first multichassis multiterabit router, the CRS-1, by Cisco Systems in 2004 was a massive effort with a correspondingly massive result. Subsequent terabit router platforms like the Juniper T1600 and the Alcatel-Lucent 7670 highlight the real need in the market for ultra-high-capacity systems, and that need can only be increasing as internet traffic grows by around 60% every year.

However, the accumulated experience from deploying the current generation of electronic core routers has also revealed their deficiencies. Practical issues of prime concern are proving to be the considerable space and electrical power that these systems require as well as the large quantities of heat that they generate.

The “magic” number is 10; this is the amount of power in kilowatts that an operator can actually supply and dissipate per rack of equipment. In cooking terms, this is the same amount of power required by an electrical grilling machine of size $132 \times 57 \times 180 \text{ cm}^3$ with nine meat skewers and a total capacity of 30 chickens. Router or grilling machine? Let’s see what we’ve got...

The CRS-1, for example, is an impressive routing system with 40 Gbit/s line-cards and a whopping 640 Gbit/s of aggregate switching capacity per chassis (or 1.2 Tbit/s counting both ingress and egress ports as Cisco does). The system occupies $213 \times 60 \times 91 \text{ cm}^3$, consumes 10.92 kW of power and weighs 723 kg – so we have already reached the “grilling” limit.

To address the scalability problem (we need routers that can grow since traffic continues to grow), the system employs multishelf configurations, but at the expense of nonlinear increases in size, weight and power consumption. Just calculate how many chickens you can grill by consuming 0.86 MW – this is the amount of power required for a 46 Tbit/s (92 Tbit/s) system to operate, comprising a total of 80 racks of equipment: 72 line-card racks and eight switching fabrics.

Let there be light

Optical communications have revolutionized the telecoms world: a single optical fibre can transport more than 25 Tbit/s using advanced modulation, multiplexing and amplification techniques. But although they have been the dominant choice for optical transport for many decades, photons have not yet found a place in the innards of core router systems.

Optical signal processing and, more generally, “switching light with light” at ultra-high speeds has been the focus of research for many years. The potential advantages in “going photonic” include low power consumption, smaller device footprint, ultra-high-speed serial operation and data format transparency. First things first, let’s see what an optical router might look like and then examine if we can actually make it small, fast and power efficient.

The basic recipe for merging electronics and photonics in optical networks is called optical packet switching. Figure 1 illustrates the proposed architecture for a photonic wavelength router, which consists of an optical routing plane and an electronic control plane. This design is based on the optical routing of high-speed data with the electronic processing of low-rate optical labels – hence it is also referred to as an optical label-switched router.

This hybrid router solution, which contains both electrical and optical functions, is the first logical step towards photonics finding their way into future commercial routing systems. The architecture balances



Perfect partners: the BOOM consortium consists of high-tech firms and academic institutions. Coordinated by the National Technical University of Athens (NTUA), the consortium includes European firms (AMO and LioniX), one telecoms operator (Telecom Italia) and three universities (the Technical University of Berlin and Technical University of Eindhoven) and three research centers.

the maturity of optical components technology against the degree of intelligence that can be achieved in the optical layer.

In this architecture, the label processing and decision making required for the intra-node routing of the packets is undertaken by FPGA-based electronic controllers. Having recognized incoming labels, the FPGA controller performs the necessary routing function with the aid of a look-up table. Depending on the label value, a suitable electrical signal is generated and

Optical router takes shape



skilled organizations with a good track record in the field. Technical University of Athens (above), participants include two telecom Italia), two more universities (Technical University of Athens, HHI, IMEC and IHP Microelectronics).

used to drive a laser diode that emits at a specific wavelength. The continuous-wave optical signal emitted is then used to drive the wavelength converter. In this way, the incoming packets are (all-optically) converted to a different wavelength according to the information embedded into the optical label – thus wavelength-based internal routing is achieved.

Naturally, there are also alternative and more futuristic “recipes” that can be used for developing all-optical routers, such as

PHOTONIC TERABIT ROUTER

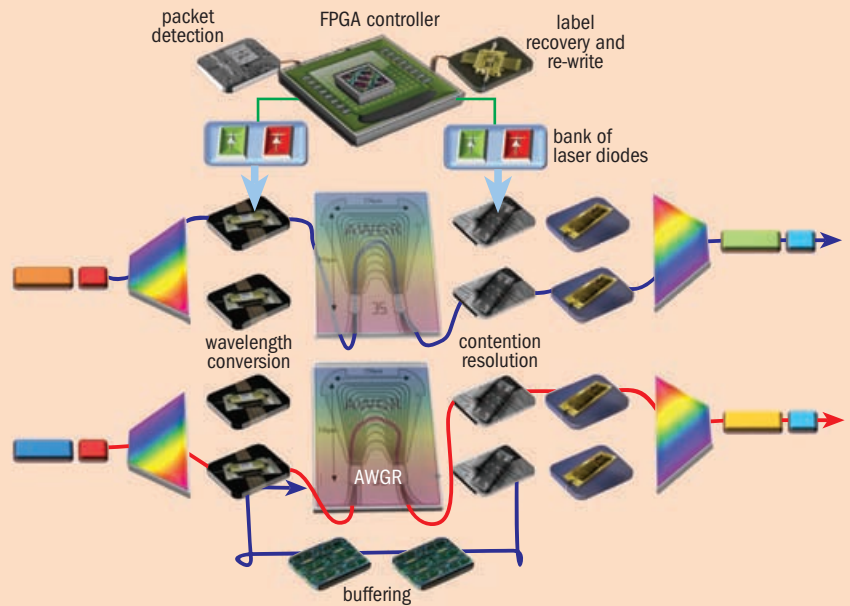


Fig. 1: in this depiction of a photonic terabit router architecture, the red and blue lines indicate the path of two incoming packets travelling through wavelength converters, arrayed waveguide grating router (AWGR), optical switches, delay lines and 2R/3R regenerators.

The routing plane is constructed using optical components and includes six main stages:

- A wavelength demultiplexer at the front end to separate incoming packets.
- The wavelength-conversion stage, which assigns a new wavelength to each packet according to the routing information

embedded in the corresponding label.

- The arrayed waveguide grating router – a passive multichannel device that routes packets according to their wavelength.
- The contention resolution stage, which typically includes all-optical wavelength converters, space switches and optical buffers to

resolve packet congestion in three dimensions – time (buffering), wavelength and space (deflection routing).

- The regeneration stage, consisting of 2R and/or 3R regenerators to compensate transmission and switching impairments.
- a WDM multiplexing stage at the back end of the router.

all-optical label switching. In such architectures, even the label/header processing is performed in the optical layer using optical logic. Label processing in the optical domain can be performed using XOR/AND optical logic gates, and packet-level control signals for routing can be generated using optical memory elements, such as optical flip-flops.

There are two main challenges with the more futuristic approaches: the extremely high number of integrated optical switches

required, and the development of all-optical random access memory capable of storing and retrieving the label values – i.e. the optical counterpart of the look-up table.

However, the implementation of any optical router architecture requires the existence of a “toolkit” that is capable of providing the following basic set of components: highly integrated wavelength converters, optical logic gates capable of high-speed processing, compact multichannel AWG circuits, integrated

buffers, and packet-capable optical regenerators. From these basic components it will be possible to create optical ASICs, i.e. customized photonic circuits that can deliver specific functionalities.

In this context, the million-dollar question is: "Is there an enabling technology?" Or, to put it another way, is there a technology platform that can easily provide all the necessary high degrees of compactness, cost-effectiveness and customization?

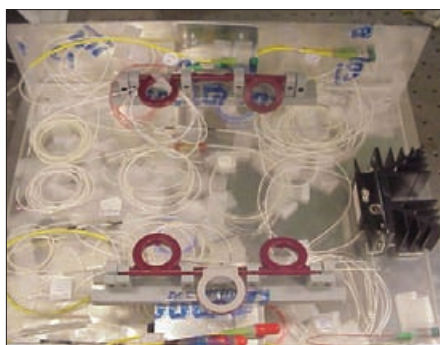
Rollercoaster ride

System-level research and development of optical signal processing is evolving at astounding rates. In the early stages of our research back in the late 1990s, a single all-optical switch, which we like to think of as the equivalent of the electronic transistor, occupied a 2 U, 19 inch rack case and seemed more like a "spaghetti dinner course" than a sophisticated piece of equipment. Appearances aside, this ultra-fast nonlinear interferometer could switch serial 40 Gbit/s data with switching energies as low as a few femtoJoules. At that time the enabling technology – photonic integration – was not ready, though we already had sufficient proof that photons could perform exceptionally well.

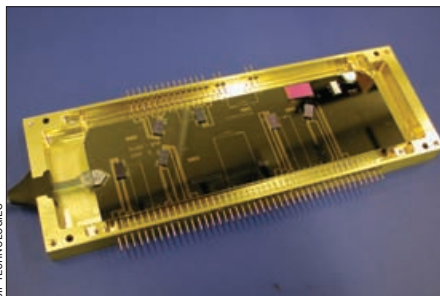
The rollercoaster ride of photonic integration in Europe started with the European project IST-MUFINS, which ran from September 2004 to August 2007, and was coordinated by the Institute of Communications and Computer Systems at the National Technical University of Athens (NTUA) in Greece. Working with the UK's Centre for Integrated Photonics (CIP), the project developed a number of components, including the first quadruple array of switches on a single chip, using a passive-assembly, hybrid integration technology.

The nonlinear elements used in the switches were indium-phosphide-based semiconductor optical amplifiers (SOAs). Photons travelling through these amplifiers interact with each other, leading to all-optical switching. These millimetre-scale SOAs are then placed on a precision-machined submount fabricated from silicon, which is then flip-chipped onto a silica-on-silicon motherboard that is responsible for guiding the light through the device. The complete packaged device occupies $90 \times 32 \times 12 \text{ mm}^3$, requires only 12 W of electrical power and achieves an aggregate throughput of 160 Gbit/s.

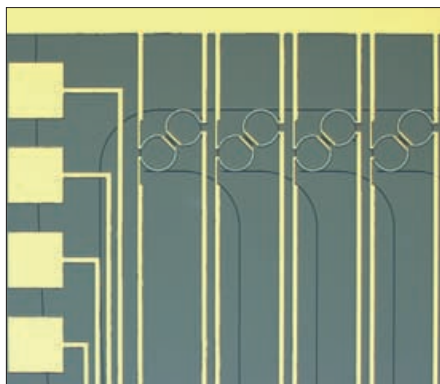
These devices allowed research to progress from single-gate optical logic elements with limited intelligence to com-



Optical spaghetti: a "packaged" optical gate built using bulk components and optical fibres, produced by the Photonics Communications Research Laboratory/ NTUA.



Tasty chips: this hybrid integrated 40 Gbit/s 3R burst-mode receiver was developed under the umbrella of the IST-MUFINS project.



Recipe for success: these micro-ring resonator circuits fabricated by LionIX/ XiO Photonics form the basis of a fully reconfigurable wavelength-routing cross connect.



Up close: the coupling region of a micro-ring resonator using silicon-on-insulator technology, as fabricated by AMO GmbH.

plex multigate optical integrated circuits. As a result, it was possible to develop new optical systems that performed various demanding networking functionalities with 40 Gbit/s packet-based data streams. Using these switches, IST-MUFINS showed that it is indeed possible to design and build large and complex processing systems that use only photons for switching photons with a record number of 12 fibre-interconnected optical switches.

Having proved the system-level feasibility of these all-optical processing systems, research then focused on producing true systems on chips, which contained on-chip interconnections of multiple photonic elements. Researchers from NTUA and engineers from CIP worked closely together to transfer the fibre-based system design into a fully integrated photonic system-on-chip: the result was the 40 Gbit/s all-optical 3R burst mode regenerator prototype. This optical ASIC can perform packet equalization, clock recovery and data regeneration of 40 Gbit/s bursty packet traffic.

An international effort

There has also been tremendous investment in photonic terabit routing systems on the other side of the Atlantic. From 2004 onwards, more than \$30 m (€23.2 m at today's exchange rate) has been invested in forward-looking projects such as IRIS and LASOR. Within these projects researchers have been working intensively to squeeze as much functionality as possible into photonic integrated chips made from indium phosphide.

For example, the IRIS project, led by Lucent Technologies Bell Labs (as it then was) and funded by the Defence Advanced Research Projects Agency (DARPA) Microsystems Technology Office (MTO), achieved the first monolithic integrated 2×8 wavelength switch, which integrates two eight-channel lasers that drive two optical switches (SOA-based interferometers), i.e. 22 SOAs on a single chip.

In the meantime, the LASOR project, led by the University of California Santa Barbara and also funded by DARPA MTO, has presented the first multifunctional photonic ASIC by integrating a tunable laser, an optical switch with on-chip amplifiers and an electro-absorption modulator on a single chip that performs data wavelength conversion at 40 Gbit/s and label rewrite at 10 Gbit/s.

The realization of highly integrated multifunctional optoelectronic chips – such as multiwavelength lasers integrated with optical switches and modulators, high

channel count integrated AWG routers, and amplified integrated delay lines – is clear evidence that photonics will have a vital role to play in the development of new transmission and switching equipment.

These projects have shown the potential of indium-phosphide fabrication. More recent developments have shown that silicon will also have an important part to play because it has the potential to provide cost-effectiveness, miniaturization,

advanced fabrication capabilities and, of course, CMOS compatibility. The hybrid assembly of indium-phosphide dies on silicon-on-insulator (SOI) wafers bearing small and low-loss waveguides has created a new and powerful recipe that has been labelled “silicon photonics”.

In this context it looks as if silicon photonics also has the ability to increase the capacity of carrier routing systems while at the same time reducing their physi-

cal size and power consumption. New research efforts are under way with the aim of developing highly integrated, silicon photonic components that will enable data switching and routing at line rates beyond 100 Gbit/s.

The European research project BOOM, which is funded under the European Commission’s 7th Framework programme (FP7), is developing new fabrication techniques for mounting the complete family of active components (lasers, photodiodes and SOAs) on SOI boards together with small-size, low-loss passive components (micro-ring resonator filters and AWGs). This new and powerful SOI optical board technology will be able to blend the cost-effectiveness and integration potential of silicon with the high bandwidth and processing power of a III-V material.

A new generation

In terms of component development, BOOM aims to provide a new generation of functional and miniaturized photonic components capable of breaking the speed limits reported so far using integrated devices, and to enable the development of compact, ultra-high-capacity photonic routers. Specifically, BOOM is developing:

- The first silicon photonic wavelength converter array chip with a record bit-rate capability of 160 Gbit/s per converter and a total switching capacity of 640 Gbit/s.
- A compact, eight-channel, ultra-dense WDM InAlAs-InGaAs photoreceiver with record high responsivity for detecting high-speed optical labels.
- A tunable and fully reconfigurable switching matrix based on micro-ring resonator technology for wavelength routing of high-speed optical packets.

This new generation of photonic components will be used to demonstrate the first photonic wavelength routing prototype with a total capacity of 640 Gbit/s, which will be capable of switching four 160 Gbit/s line-rate channels, consuming power equal to some 10s of Watts and occupying space as small as a 4U rack-mount case. BOOM officially started in May 2008 and the system integration of its first prototype switch is expected in the first quarter of 2011. ●

● For more information visit <http://mufins.cti.gr> and www.ict-boom.eu.

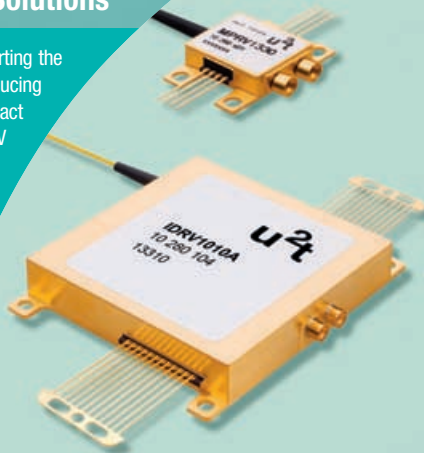
Leontios Stampoulidis and Efstratios Kehayas are senior researchers at the Photonics Communications Research Laboratory, National Technical University of Athens, Greece (www.telecom.ece.ntua.gr/photronics/).



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